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# Voltage-Dependent Charge Storage in Cladded $Zn_{0.56}Cd_{0.44}Se$ Quantum Dot MOS Capacitors for Multibit Memory Applications

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As conventional memories approach scaling limitations, new storage methods must be utilized to increase Si yield and produce higher on-chip memory density. Use of II–VI $Zn_{0.56}Cd_{0.44}Se$ quantum dots (QDs) is compatible with epitaxial gate insulators such as ZnS-ZnMgS. Voltage-dependent charging effects in cladded $Zn_{0.56}Cd_{0.44}Se$ QDs are presented in a conventional metal–oxide–semiconductor capacitor structure. Charge storage capabilities in Si and ZnMgS QDs have been reported by various researchers; this work is focused on II–VI material $Zn_{0.56}Cd_{0.44}Se$ QDs nucleated using photoassisted microwave plasma metalorganic chemical vapor deposition. Using capacitance–voltage hysteresis characterization, the multistep charging and discharging capabilities of the QDs at room temperature are presented. Three charging states are presented within a 10 V charging voltage range. These characteristics exemplify discrete charge states in the QD layer, perfect for multibit, QD-functionalized high-density memory applications. Multiple charge states with low operating voltage provide device characteristics that can be used for multibit storage by allowing varying charges to be stored in a QD layer based on the applied "write" voltage.

**Key words:** II–VI quantum dots, multi-bit memory, capacitance-voltage characterization, quantum dot super lattice, hysteresis

## INTRODUCTION

The demand for small memory devices has led the industry to pursue many innovations in conventional memory devices such as high-$\kappa$-dielectric tunnel oxide insulators in an attempt to scale down existing memory designs. Memory scaling innovation lags behind conventional complementary metal–oxide–semiconductor (CMOS) technology, and the current minimum feature size is 12 nm with gate oxide thickness of 0.8 nm.[1] CMOS logic can operate at threshold voltages lower than memories, further compounding the need for small and efficient memory. Unlike $SiO_2$ and $HfO_2$ insulator thin films, use of II–VI tunnel insulators such as lattice-matched ZnS-ZnMgS enables high-$\kappa$ gates with low interfacial charge. Use of II–VI quantum dots (QDs) is compatible with epitaxial gate insulators such as ZnS-SnMgS. Various other II–VI QD compositions such as ZnSeTe-ZnSe can be utilized instead of $Zn_{0.56}Cd_{0.44}Se$. Dynamic random-access memory scaling suffers from large capacitors required for data storage, and static random-access memory cannot provide high chip density since a cell contains four to six transistors.[1] Engineering a new storage method in conventional memory structures would allow higher yield and high on-chip memory density. Going beyond scaling, functionalizing conventional memory structures with QDs can provide multibit storage while maintaining low energy consumption, high-lifetime charge storage, and exceptional data storage density. QDs offer high potential for memory applications due to the effective confinement of holes.[2] The application of QDs in memory structures will allow engineers to overcome the size limitations in memory design. The QD superlattice (QDSL) provides higher exciton binding energy, minibands, and a large discrete density of

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