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Failure Analysis of Board-Level Sn-Ag-Cu Solder Interconnections Under JEDEC Standard Drop Test

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This work investigates the board-level drop reliability of printed circuit boards (PCBs) assembled using three chip-size packages subjected to Joint Electron Device Engineering Council (JEDEC) standard drop test condition B. The acceleration and dynamic strain responses at several locations of the board-level package in the time and frequency domain are comprehensively investigated. The results in the time domain suggest that the dynamic response of the board-level package has two phases: forced vibration and free vibration. The maximum response occurs at the first half free vibration cycle. The acceleration response at the center of the PCB is larger than at the edges, whereas the dynamic strain response is just the opposite. The results in the frequency domain show that the first mode is fundamental. In addition, failure analysis is performed using the dye-and-pry test and cross-section test, suggesting that the brittle cracking occurs at the layer between the integrated circuit (IC) pad and the solder, not only through intermetallic compound (IMC) but also along the surface between the IC pad and IMC.

Key words: Dynamic responses, time domain, frequency domain, failure analysis, intermetallic compound

INTRODUCTION

The miniaturization of portable electronic products causes frequent drops during transportation or usage. Meanwhile, the multiple functions of portable electronic products make the integrated circuit (IC) package smaller. Moreover, the strain rates of solder joints under drop testing are higher than those under thermal cycling or other mechanical loads. Compared with lead-containing solders, lead-free solders are in general stiffer and more brittle. This makes such smaller lead-free solder joints more susceptible to shock loads compared with lead-containing solder joints.[1] Therefore, it is necessary to study the dynamic response of board-level packages and the failure mechanism of lead-free solder joints during drop testing.

Liu et al.[2] and Lim et al.[3] presented studies on the product-level drop test which suggested that this test is complicated due to its dependence on various factors (e.g., drop orientation and product design). Thus, it is difficult to evaluate the drop performance of solder joints by product-level drop testing. To standardize the test board and test methodology and provide reproducible assessment of drop test performance of surface-mounted components, the Electronic Industries Alliance (EIA) has published two Joint Electron Device Engineering Council (JEDEC) standards: JESD22-B110A[4] and JESD22-B111[5] for the subassembly mechanical shock test and the board-level drop test of handheld electronic products, respectively. Following this guidance, the acceleration and strain response of the test board, and the number of drops until failure for each component are to be monitored during the board-level drop test, in addition to product-level drop testing.

The number of drops until failure, crack location, and crack characteristics of solder joints depend on the dynamic stress and strain response (e.g., stress distribution, stress magnitude, and strain rate) of solder joints to a certain extent during the

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