Journal of ELECTRONIC MATERIALS, Vol. 42, No. 11, 2013
DOI: 10.1007/s11664-013-2773-y

Design of Dislocation-Compensated ZnS_ySe_{1-y}/GaAs (001) Heterostructures

T. KUJOFSA[1,2,3] and J.E. AYERS[1]

1.—Electrical and Computer Engineering Department, University of Connecticut, 371 Fairfield Way, Unit 4157, Storrs, CT 06269-4157, USA. 2.—e-mail: Tedi.Kujofsa@gmail.com. 3.—e-mail: Tedi.Kujofsa@engr.uconn.edu

The understanding of lattice relaxation and dislocation dynamics in lattice-mismatched semiconductors makes it possible to design metamorphic device structures utilizing the dislocation compensation mechanism for reduced defects, improved performance, and enhanced reliability. We have developed a dislocation dynamics model accounting for misfit–threading interactions and have applied it to ZnS_ySe_{1-y}/GaAs (001) heterostructures.[1] Dislocation compensation involves the removal of threading dislocations associated with one sense of misfit dislocations by bending them over to create misfit dislocations of the opposite sense at an intentionally mismatched interface. Here we investigated the design of dislocation-compensated ZnS_ySe_{1-y}/GaAs (001) heterostructures and considered the sulfur mole fraction tolerances applicable to such structures. We considered two types of structures: type A involved a uniform-composition (ungraded) layer on top of a uniform-composition buffer, while type B involved a uniform-composition layer on a linearly graded buffer. For each structure type we studied the requirements on the thickness and compositional profile of the buffer layer to optimize the removal of mobile threading dislocations from the top uniform (device) layer as well as the allowed tolerance in compositional overshoot to achieve structures with low threading dislocation density. We show for both types of structure that (i) for given compositional overshoot at the buffer–device layer interface, there is an optimum buffer thickness which minimizes the dislocation density; and (ii) for given buffer thickness there is an optimum overshoot which minimizes the dislocation density.

Key words: Relaxation, dislocation compensation, linearly and ungraded buffers, compositional tolerance

INTRODUCTION

The implementation of metamorphic semiconductor devices requires control of the dislocation density threading through the device layers. Recently we reported the mechanism of dislocation compensation, which we define as removal of threading dislocations associated with one sense of misfit dislocation by bending them over to create misfit dislocations of the opposite sense. We can arbitrarily assign positive and negative sense to dislocations which relax compressive and tensile strain, respectively. Qualitatively, a compressive (tensile) interface can be used for dislocation compensation in a structure with a tensile (compressive) buffer. Design of such a dislocation-compensated semiconductor heterostructure device requires a dislocation dynamics model which accounts for (i) the time evolution of kinetically limited strain relaxation, (ii) thermal activation of glide, and (iii) misfit–threading dislocation interactions. Several kinetic models have been proposed by Matthews et al.,[2] Dodson and Tsao,[3] Houghton,[4] Sasaki et al.,[5] and Horbaschk et al.[6] which account for thermally activated glide of preexisting dislocations,[1] dislocation

(Received December 17, 2012; accepted September 7, 2013; published online October 8, 2013)