Journal of ELECTRONIC MATERIALS, Vol. 42, No. 7, 2013
DOI: 10.1007/s11664-012-2287-z

Power Factor Characterization of Ge/SiGe Thermoelectric Superlattices at 300 K

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To accurately characterize the efficiency of thermoelectric materials and characterize the maximum power that they can produce, a device using micro/nanofabrication techniques has been developed, enabling all three properties included in the figure of merit, ZT, of a thermoelectric material to be measured using a single device. The fabrication and testing of the device are presented. The electrical conductivity and Seebeck coefficient of Ge/SiGe heterostructures grown by low-energy plasma-enhanced chemical vapor deposition are used for demonstration. Experimental results as a function of quantum well width are presented, demonstrating power factors up to 6.02 ± 0.05 mW m^{-1} K^{-2} at 300 K. Modeling and physical characterization demonstrate that these results are presently limited by high threading dislocation density.

Key words: Thermoelectrics, electrical conductivity, Seebeck coefficient, power factor, device fabrication, SiGe

INTRODUCTION

Thermoelectric materials have the ability to covert heat into electricity via the Seebeck effect, or to produce cooling using electricity by the Peltier effect. Harvesting waste heat is becoming an attractive alternative for many companies that want to improve the efficiency of their systems. The efficiency of a thermoelectric material is quantified by its figure of merit, defined as $ZT = \alpha^2\sigma T/\kappa$, where α is the Seebeck coefficient, σ is the electrical conductivity, and κ is the thermal conductivity.[1] Good thermoelectric materials require high electrical conductivity and Seebeck coefficient combined with low thermal conductivity. The numerator of the figure of merit is called the power factor, $\alpha^2\sigma$, which determines the maximum power available from a material.

(Received July 7, 2012; accepted September 25, 2012; published online November 10, 2012)

Commercial thermoelectric modules are typically produced using Bi_2Te_3/Sb_2Te_3 bulk alloys with $ZT \approx 1$ at T = 300 K. However, these materials are rare and cannot be integrated with complementary metal–oxide–semiconductor (CMOS) electronic circuits used in autonomous systems.

For three-dimensional (3D) materials, the Wiedemann–Franz law provides a limit to the maximum ZT that can be achieved, as σ and κ are linked by this law. Optimizing the figure of merit therefore becomes challenging, since improving one thermoelectric parameter normally degrades another. As proposed by Hicks and Dresselhaus,[2] low-dimensional structures could potentially have higher figures of merit. Multilayer superlattices have already demonstrated enhanced ZT values compared with bulk materials, since the electrons or holes are confined to move in two dimensions and a multilayer structure may contribute to the reduction in thermal conductivity by scattering phonons at interfaces.[1]

SiGe heterostructures of 10 μm thickness based on bulk Ge quantum wells (QWs) and SiGe alloy barriers