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Design of S-Graded Buffer Layers for Metamorphic ZnS_ySe_{1-y}/GaAs (001) Semiconductor Devices

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We present design equations for error function (or "S-graded") graded buffers for use in accommodating lattice mismatch of heteroepitaxial semiconductor devices. In an S-graded metamorphic buffer layer the composition and lattice mismatch profiles follow a normal cumulative distribution function. Minimum-energy calculations suggest that the S-graded profile may be beneficial for control of defect densities in lattice-mismatched devices because they have several characteristics which enhance the mobility and glide velocities of dislocations, thereby promoting long misfit segments with relatively few threading arms. First, there is a misfit-dislocation-free zone (MDFZ) adjacent to the interface, which avoids dislocation pinning defects associated with substrate defects. Second, there is another MDFZ near the surface, which reduces pinning interactions near the device layer which will be grown on top. Third, there is a large built-in strain in the top MDFZ, which enhances the glide of dislocations to sweep out threading arms. In this paper we present approximate design equations for the widths of the MDFZs, the built-in strain, and the peak misfit dislocation density for a general S-graded semiconductor with diamond or zincblende crystal structure and (001) orientation, and show that these design equations are in fair agreement with detailed numerical energy-minimization calculations for ZnS_ySe_{1-y}/GaAs (001) heterostructures.

Key words: Metamorphic buffer, S-graded, energy minimization, ZnSSe/GaAs (001), equilibrium strain, misfit dislocation density

INTRODUCTION

Metamorphic or partly lattice-relaxed semiconductor devices are of great interest because their use removes the compositional constraints associated with pseudomorphic design, enabling the use of lattice-mismatched materials with a wide range of desirable properties such as energy gap, low-field mobility, and carrier saturation velocity. An example is the AlGaAs/InGaAs high-electron-mobility transistor (HEMT) on a GaAs substrate, for which pseudomorphic design places an upper limit of 25% on the indium mole fraction, but higher indium content is desirable to achieve better direct-current (DC) and high-frequency transistor performance. Metamorphic devices which have been fabricated on lattice-mismatched substrates include InGaAs/InAlAs HEMTs on GaAs,[1] InGaAs/InAlAs heterojunction bipolar transistors (HBTs) on GaAs,[2] InGaAs/InP HEMTs and HBTs on GaAs,[3] InAlAs photodiodes on GaAs,[4] InAsSb/AlInAsSb light-emitting diodes on GaSb,[5] AlInGaAsSb laser diodes on GaSb,[6] InGaAs/InAlGaAs laser diodes on GaAs,[7] InGaAsSb/InAlAs quantum cascade laser structures on GaAs,[8] and InAlAs solar cells on GaAs.[9] Most experimental and modeling studies have focused on metamorphic structures with linearly graded buffer layers.[1–6,10–28]

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