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Relaxation Dynamics and Threading Dislocations in ZnSe and ZnS_ySe_{1-y}/GaAs (001) Heterostructures

T. KUJOFSA,[1,2,3] S. CHERUKU,[1] W. YU,[1] B. OUTLAW,[1] S. XHURXHI,[1] F. OBST,[1] D. SIDOTI,[1] B. BERTOLI,[1] P.B. RAGO,[1] E.N. SUAREZ,[1] F.C. JAIN,[1] and J.E. AYERS[1]

1.—Department of Electrical and Computer Engineering, University of Connecticut, 371 Fairfield Way, Unit 4157, Storrs, CT 06269-4157, USA. 2.—e-mail: Tedi.Kujofsa@gmail.com. 3.—email: Tedi.Kujofsa@engr.uconn.edu

The design of lattice-mismatched semiconductor devices requires a predictive model for strains and threading dislocation densities. Previous work enabled modeling of uniform layers but not the threading dislocations in device structures with arbitrary compositional grading. In this work we present a kinetic model for lattice relaxation which includes misfit–threading dislocation interactions, which have not been considered in previous annihilation–coalescence models. Inclusion of these dislocation interactions makes the kinetic model applicable to compositionally graded structures, and we have applied it to ZnSe/GaAs (001) and ZnS_ySe_{1-y}/GaAs (001) heterostructures. The results of the kinetic model are consistent with the observed threading dislocation behavior in ZnSe/GaAs (001) uniform layers, and for graded ZnS_ySe_{1-y}/GaAs (001) heterostructures the kinetic model predicts that the threading dislocation density may be reduced by the inclusion of grading buffer layers employing compositional overshoot. This "dislocation compensation" effect is consistent with our high-resolution x-ray diffraction experimental results for graded ZnS_ySe_{1-y}/GaAs (001) structures grown by photoassisted metalorganic vapor-phase epitaxy.

Key words: Plastic flow, relaxation dynamics, threading dislocation, dislocation compensation, graded layers, metamorphic devices

INTRODUCTION

The design of lattice-mismatched semiconductor device structures requires a predictive model for strains and threading dislocation densities, which are important in determining device performance and reliability. Previous work enabled modeling of single heterostructures but not compositionally graded structures of the types used in mesomorphic transistors and light-emitting diodes. In this work we present a kinetic model for lattice relaxation in semiconductor heterostructures which accounts for misfit–threading dislocation interactions and therefore can be applied to partially relaxed device structures employing compositional grading and mismatched interfaces.

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ANNIHILATION–COALESCENCE MODELS

For uniform-composition heteroepitaxial layers on mismatched substrates, it is often observed that the threading dislocation density is inversely proportional to the layer thickness, for layers which are much greater than the critical layer thickness and therefore nearly relaxed at the growth temperature.[1] This behavior has been reported for ZnSe/GaAs,[2,3] InAs/GaAs,[4] GaAs/InP,[4] InAs/InP,[4] and GaAs/Si.[5] Tachikawa and Yamaguchi[6] devised a semiempirical model for the threading dislocation density in a uniform, nearly relaxed heteroepitaxial layer which was based on annihilation and coalescence of threading dislocations. The differential equation governing the threading dislocation density D was assumed to be

$$\frac{dD}{dy} = -C_1 D - C_2 D^2, \quad (1)$$