Applied Thermal Engineering 36 (2012) 181–187

Contents lists available at SciVerse ScienceDirect

Applied Thermal Engineering

journal homepage: www.elsevier.com/locate/apthermeng

Thermal conduction analysis and characterization of solder bumps in flip chip package

Xiangning Lu [a], Tielin Shi [b], Qi Xia [a], Guanglan Liao [a,*]

[a] State Key Laboratory of Digital Manufacturing Equipment and Technology, Huazhong University of Science and Technology, Wuhan, Hubei 430074, PR China
[b] Wuhan National Laboratory for Optoelectronics, Wuhan, Hubei 430074, PR China

ARTICLE INFO

Article history:
Received 19 August 2011
Accepted 17 December 2011
Available online 22 December 2011

Keywords:
Flip chip
Solder bump
Defects
Heat transfer
Thermal resistance

ABSTRACT

Flip chip has been widely used in microelectronic packaging to meet the requirements of high density and optimal performance. With the shrinking of the package size, the heat dissipation problem is getting more serious, and the thermal modeling and measurement of flip chip have become hot topics. This paper investigated the thermal performance of the solder bumps using analytical and numerical methods. A lumped thermal resistance network was derived from the mathematical model of heat transfer in the flip chip structure. Common defects were introduced in the 3D finite element model. The impact of the defects on the heat conduction was investigated by the temperature distribution. The thermal performance of the solder bumps was characterized by using the thermal resistances. The relationship between the thermal resistance and the defects size was also studied, and the finite element model describes well the experimental data available from the literature. The results demonstrate that this model is effective for the thermal characterization of solder bumps, and can provide guidelines for failure detection in flip chip package.

1. Introduction

Surface mounting technology plays an increasingly important role in microelectronic packaging. Flip chips (FC), ball grid array (BGA) and chip scale packages (CSPs) have been extensively used, in which solder bumps or solder balls are employed to interconnect the chip/package and the substrate. The solder bump technology provides decreased package size, greater I/O density and larger speed of signal propagation [1,2]. As the package scale continues to shrink, the chip power density increases dramatically, and the heat dissipation becomes a significant problem [3]. The inclusion of low-k materials also makes the situation deteriorate further. Excessive heat and large temperature gradients may introduce failures in the components [4]. Therefore, thermal modeling and measurement of flip chip packages have become hot topics recently in structure design and package reliability evaluation.

Thermal resistance is a principal index that indicates the thermal dissipation capability and is usually determined experimentally using an infrared (IR) technique, although the JEDEC electrical test method based on the JESD51-1 specification may also be used [5,6]. Due to the complexity of experiments for measuring thermal resistances, the finite element method (FEM) and finite volume method (FVM) are widely used in numerical analysis to perform thermal evaluation of the flip chip package. Chen et al. [7] proposed a finite element numerical methodology to predict the thermal resistance of FC-PBGA package, in which the empirically determined coefficients for convective heat transfer were applied on different exposed surfaces. Kandasamy et al. [8] constructed a CFD-based thermal model to investigate the thermal performance of the FC-CBGA package with and without a lid both in natural and forced convection environments. Joiner et al. [9] compared the thermal performances of flip chip packages between the plastic laminate substrate and ceramic substrate using finite element analysis. However, in these research the chip is regarded as a node, and the thermal resistances of junction-to-case, junction-to-board and junction-to-ambient are used to characterize the thermal performance of a given device package, as depicted in Fig. 1, while the internal structure of the package is neglected and the heat conduction via solder bumps or solder balls are not taken into consideration.

This study focused on the heat transfer analysis and thermal characterization of the solder bumps in flip chip package. The mathematical model of heat transfer in the flip chip structure is devised. A lumped thermal resistance network is derived from the simplified analytical model and the finite element method is used to evaluate the thermal performance of the solder bumps. The numerical code of COMSOL Multiphysics is adopted to perform the

* Corresponding author. Tel.: +86 27 87793103; fax: +86 27 87792413.
E-mail address: guanglan.liao@mail.hust.edu.cn (G. Liao).

1359-4311/$ – see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.applthermaleng.2011.12.028