

K N Toosi University of Technology Faculty of Electrical Engineering Center of Excellence in Computation and Characterization of Devices and Subsystems The Second Iranian Conference on Engineering Electromagnetics (ICEEM 2014), Jan. 8-9, 2014



## **On-chip Silicon Light Emitters for Surface Plasmon Polariton Generation in CMOS Technology**

M. A. Karami<sup>\*</sup>, A. Amiri Sani, and M. H. Ghormishi

Department of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran

\*Corresponding author: <u>karami@iust.ac.ir</u>

ABSTRACT— On-chip point and line source photon emitters realized in 0.35 µm standard CMOS silicon technology are introduced in this paper. The dedicated photon emitters are designed and implemented for the surface plasmon polariton (SPP) generation on standard Integrated Circuits (IC). The photon emission occurs by hot carrier relaxation as the main physical process. The photon emitters realized with standard silicon **CMOS** technology free from complex are semiconductor materials and metals.

**KEYWORDS:** CMOS technology, Light emitter, Silicon.

## I. INTRODUCTION

Since the development of the first bipolar junction transistor in Bell labs in 1947, transistors have been scaled following the Moore's law with the number of transistors doubling on the same size chip in every 18 Nowadays state-of-the-art months [1]. transistors have gate sizes of about 16nm and the miniaturization of transistors is in progress [2]. The ultimate limit of scaling in electronics is set by a few silicon atoms which can be controllable by the metal gate [3]. Working with transistors which have a few atoms, is a new regime of operation where the quantum transport should be studied [4]. Several candidates are considered for replacing electrons in Integrated Circuits (ICs) to increase the speed of operation and the bandwidth [5].

The manipulation of the quantas of light named as photons for data processing has been underway for several years in the field of photonics. The main obstacle for replacing the electronic transistors with the optical ones is the fundamental restriction of diffraction limit in optics which forces the optical devices to be at least a wavelength of the light in size [6]. Several structures were proposed with half the wavelength size which ends in leaking out the light and less localization [7]. Surface Plasmon Polaritons (SPP) are the electron waves present at the surface of metals. SPPs propagate at the interface of metals and dielectrics and two main structures (MIM, and IMI) are regarded as the plasmonic waveguides as shown in Fig. 1 [8].



Fig. **1** The main plasmonic waveguide structures: Metal-Insulator-Metal (MIM), and Insulator Metal Insulator (IMI). The IMI structure in the figure consists of the air at top, gold in the middle and substrate (a dielectric) at the bottom, and the MIM structure consists of two metal sheets surrounding a dielectric in between.