Design of two 9 transistors Low consumption SRAM cell with improved fastness and stability

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Abstract

One of the most important blocks in today's digital systems are SRAM memory blocks, because these blocks are widely used as a memory cache in different types of microprocessors. Power consumption of SRAM cell consists of two components of leakage power (static) and dynamic power. Due to high volume of these cells in today's microprocessors, their leakage power is very important. Data stability and static noise margin (SNM) in the SRAM cells with respect to reduction of supply voltage is gaining more attention. In addition to consumed power and data stability, reading and writing delay of SRAM cells has a main role to improve fastness and performance of microprocessors. In this paper, two new designs of 9 transistors cells has been proposed that are compared with four different cells with 6, 7, 8 and 9 transistors addressed in the recent literature. Simulation results show that dynamic and static power consumption of these proposed two cells are less than all other cells that are previously presented and are also faster than 6, 7 and 8 transistors cells in both reading and writing stages.

Keywords*: Data Stability, reading and writing delay, dynamic power, leakage power.*

1. Introduction

In recent years, by increasing in mobile tools and portable devices that their required power is supplied by batteries, consumed power has became one of the most important issues in these devices and VLSI electronic systems. Therefore, electronic system design with low power consumption is one of the most challenging research topics and has raised many attentions. In many digital electronic chips high power consumption increases chip's operating temperature, reduce circuit reliability and make it difficult and expensive to cool the chip. Increase in power consumption of portable systems that use a battery as a power supply, not only decreases lifetime of the battery but also increases in operating temperature.

Today, one of the memory blocks that is vital in many digital electronic systems are the SRAM memories, because it has many applications in different types of microprocessors. For example, about 50 percent of a RISC microprocessor chip is occupied by cache memory which is SRAM [1]. Using pieces of SRAM that are digitally programmable as a memory for storing configuration information is another applications of SRAMs. For example, FPGA is one of the pieces in which each logic block is connected by a series of switch to the other logic blocks that the gates of these switches are connected to the output of a SRAM cell [2]. The main feature of SRAM memory blocks is high number of cells that are used in these blocks that greatly increases the number of transistors. For example, a quad-core itanim processor in 65 nanometers technology there are 2050 million transistors that 1420 million of those transistors belong to the cache memory which comprises about 70 percent of the total number of chip's transistors [3]. The number of transistors in this chip that is related to cache is about 3.3 times of the number of transistors used in the quad-core. Since these memories occupy a large surface of the chips, these circuits are known as high consumption circuits, so reduction in their consumption and improvement in their speed need more attention. Therefore in the recent years much studies has been carried out in this area. SRAM memories, like other digital circuit, consume static and dynamic power consumption that static power is dependent to leakage currents of the cells [4]. Three components of leakage current are below threshold leakage current, gate leakage current and link leakage current. Dynamic Power in SRAM is due to charge and discharge of capacitor during the process of reading and writing that its major part is because of changing of line voltage of bits during writing data on the cell or reading the content of memory cells [5].

This paper is the result of a research aimed at simultaneously reducing static and dynamic power and improving data stability and fastness in SRAM cells. The structure of this paper is as follows. In section two a number of previous researches in this area are briefly considered and also the seven cells is introduced in this section which four cells of these seven cells are described by simulation and others without simulation. In the third section one of the two proposed new cells are introduced and the other proposed cell is introduced in the fourth section. The