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ORIGINAL RESEARCH PAPER

A hardware centric algorithm for the best matching unit searching stage of the SOM-based quantizer and its FPGA implementation

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Abstract Parts of a self-organizing map (SOM)-based quantizer can be performed in parallel, i.e., distance calculation between an input pixel and a group of codewords or processing elements (PEs), and updating codewords. To search for the best matching unit (BMU) whose distance is the minimum, all distances are inevitably required to compare with each other. It is true that a group of comparators and registers can be instantiated with equal size to the distances (which is equivalent to the number of PEs) and performed in a multistage manner to come up with the minimum distance and its index. In this way, the algorithm requires $n = \log_2 C$ clock cycles, where C is the number of PEs and $\sum_{k=0}^{n-1} 2^k$ are the number of comparators and registers. In this paper, we propose a novel hardware centric algorithm with the objective to accelerate the BMU searching stage of the SOM-based quantizer. In a simple form, the algorithm relies on using a PE's distance as an address of a memory to store its index. Simultaneously with storing indices of all PEs, the states of all 'non-empty' addresses within the memory are prepared. In this way, it can be stated that the position of the first non-empty state corresponds to the memory address whose content is the BMU index. The approach to find the first position of the non-empty state within a single clock cycle is also detailed. The algorithm is also adapted to make it more feasible to realize on an FPGA platform. The synthesis results compared with the conventional BMU searching indicate that the FPGA resource requirements of the algorithm are 1.8 and 1.57 times in terms of slices and LUT usages, respectively. In terms of acceleration, the algorithm outperforms the conventional ones by a factor of 1.8 for a test image of size 512 × 512 pixels.

Keywords Image compression · Image quantization · Self-organizing map · Multi-port memory

1 Introduction

A true color digital image requires 24 bits to specify the color of each pixel on the screen. It is expensive to have a high-speed memory to support such a full-color display on a high resolution display. An alternative solution is to provide a limited number of bits for specifying the color of each pixel. Each of these values is then used as an index into a user-defined color palette table. The process of carrying out a color palette table selection is known as the color quantization process. The color quantization is one of the most useful lossy compression methods with the benefit of easy implementation on the image receiver site. Typically, the color quantization attempts to find an acceptable set of palette colors that can be used to represent the original colors of a digital image. There are two points that make this lossy image compression successful. First of all, it exploits the limited ability of human perception which is capable of distinguishing less than a thousand colors. In addition, it exploits the limited capability of many display devices to display true colors on many display devices like a billboard [5] or a low quality LCD (liquid crystal display) which has constantly been used as a replacement of text centric display media. Applying the color quantization to an RGB color image frame of size 640 × 480 pixels, the resulting image with a color palette size of 256 will have only (640 × 480) + (256 × 3) = 307,968 bytes which is about

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