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ORIGINAL RESEARCH PAPER

Low-latency histogram equalization for infrared image sequences: a hardware implementation

Volker Schatz

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Abstract This work describes a hardware implementation of the contrast-limited adaptive histogram equalization algorithm (CLAHE). The intended application is the processing of image sequences from high-dynamic-range infrared cameras. The variant of histogram equalization implemented is the one most commonly used today. It involves dividing the image into tiles, computing a transformation function on each of them, and interpolating between them. The contrast-limiting is modified to facilitate the hardware implementation, and it is shown that the error introduced by this modification is negligible. The latency of the design is minimized by performing its successive steps simultaneously on the same frame and by exploiting the vertical blank pause between frames. The resource usage of the histogram equalization module and how it depends on its parameters has been determined by synthesis. The design has been synthesized and tested on a Xilinx FPGA. The implementation supports substituting other dynamic range reduction modules for the histogram equalization component by partial dynamic reconfiguration.

Keywords Histogram equalization · CLAHE · Infrared images · FPGA design · Partial dynamic reconfiguration

1 Introduction

Histogram equalization is an image enhancement technique that consists in a grey-level transform designed to equalize the frequency of occurrence of different grey values. It has its origins in the information theoretic problem of maximizing the information content of discretized data by applying a transformation before discretization. These concepts were applied to images by Hummel [14]. Histogram equalization has since been successively refined. Most importantly, each pixel can be transformed based on the histogram of a contextual region [15, 17, 18, 23], and the contrast amplification can be limited by clipping the histogram [24]. The latter variant, called contrast-limited adaptive histogram equalization (CLAHE), is in most widespread use today and is the method that has been implemented here.

Specialized hardware for computing histogram equalization also has a long history. The paper that introduced contrast limiting [24] also discussed how to implement histogram equalization on special processor architectures. Since then, implementations as a specialized multiprocessor machine [8] and as parallel software on commercially available hardware [19] have been provided. More recently, several implementations of global histogram equalization have been developed that either partly [7, 26] or exclusively [3, 16, 20] rely on FPGA logic. Reza has presented a hardware implementation of CLAHE with an application in medical imaging in mind [25]. Ferguson et al. [9] have developed an FPGA implementation of CLAHE intended for video processing. Both closely follow the software algorithm.

The intended application of this implementation is the processing of image sequences from an infrared (IR) camera with a dynamic range of 14 bits or more. Reducing the dynamic range is necessary before the images can be displayed on a standard computer monitor. Most displays support a dynamic range of 8 bits in each colour channel, resulting in a dynamic range of 8 bits for greyscale images

V. Schatz (✉)
Fraunhofer Institut für Optronik,
Systemtechnik und Bildauswertung,
Gutleuthausstraße 1, 76275 Ettlingen, Germany
e-mail: volker.schatz@iosb.fraunhofer.de