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ORIGINAL RESEARCH PAPER

Efficient hardware implementation of 8 × 8 integer cosine transforms for multiple video codecs

Khan A. Wahid · Muhammad Martuza · Mousumi Das · Carl McCrosky

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Abstract The current trend of digital convergence leads to the need of the video decoder that should support multiple video standards such as, H.264/AVC, JPEG, MPEG-2/4, VC-1, and AVS on a single platform. In this paper, we present a cost-sharing architecture of multiple transforms to support all five popular video codecs. The architecture is based on a new multi-dimensional delta mapping. Here the inverse transform matrix of the Discrete Cosine Transform (DCT) of AVS, that has the lowest computational unit, is taken as the base to compute the inverse DCT matrices of the other four codecs. The proposed architecture uses only adders and shifters on a shared basis to reduce the hardware cost significantly. The shared architecture is implemented on FPGA and later synthesized in CMOS 0.18 μm technology. The results show that the proposed design satisfies the requirement of all five codecs with a maximum decoding capability of 60 fps of a full HD video. The scheme is also suitable for low-cost implementation in modern multi-codec systems.

Keywords 8 × 8 inverse integer transform · Inverse DCT · H.264/AVC · JPEG · MPEG-2/4 · VC-1 · AVS · Hardware share

1 Introduction

An evident trend in modern world is the digital convergence in the current electronic consumer products. Now-a-days, people want the portable devices to have various functions like Video on Demand (VOD), Digital Multimedia Broadcasting (DMB), Global Positioning System (GPS) or the navigation system, Portable Multimedia Player (PMP) and so on. Due to such demand, it is necessary to support the widely used video compression standards in a single system-on-chip (SoC) platform. On the other hand, integrating multiple standard encoding or decoding circuits into a single chip increases the area and power consumption, which has a negative impact on the overall system. So the goal is to find a way that the multi-codec system achieves high performance, as well as low cost.

The circuit sharing is an efficient method for the hardware cost reduction. A shared design to support multi-video codecs based on 1-D matrix mapping has been presented in [1, 2]. Several other designs based on matrix factorization to support different video codecs have been reported in [3–6]. The authors in [14, 15] have discussed a general architecture for transform and quantizer that can be applied to modern video codecs. The works exploit the similarities between the 4-point and 8-point Discrete Cosine Transform (DCT) basis matrices. The authors in [18] and [19] have presented another shared architecture to compute both 4-point and 8-point 1-D DCT for H.264 and VC-1 codecs that is based on matrix factorization and row–column permutation. The scheme can also be applied to 2-D integer transforms. Chao et al. in [16] have presented a hardware sharing architecture of 8 × 8 inverse transform for H.264 and VC-1 standards. A pipelined design to support multiple codecs (JPEG, MPEG-2, and H.264) is presented in [17] that includes transform, quantizer and zigzag scan units. In [22], the authors present a low-cost multi-mode entropy data decoder that supports multiple video coding standards. Silicon Image Inc. currently supplies a Multi-standard High-Definition Video Decoder

K. A. Wahid (✉) · M. Martuza · M. Das · C. McCrosky
Department of Electrical and Computer Engineering, University of Saskatchewan, Saskatoon, SK S7N5A9, Canada
e-mail: khan.wahid@usask.ca