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ORIGINAL RESEARCH PAPER

FPGA implementation of the JPEG2000 binary arithmetic (MQ) decoder

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Abstract A flexible FPGA implementation of the JPEG-2000 binary arithmetic decoder is presented in this paper. The proposed JPEG2000 binary arithmetic decoder reduces the amount of resources used on the FPGA allowing 19% more entropy block decoders to fit on chip and consequently increasing the throughput by 21% beyond previous designs.

Keywords JPEG2000 binary arithmetic decoder · MQ decoder · FPGA

1 Introduction

JPEG2000 is an image compression standard ratified by the Joint Photographic Expert Group (JPEG) in December of 2000 [1]. The many advantages of the JPEG2000 standard include a higher compression performance by 30% over the previous JPEG standard [2–4] and inherent features such as an embedded bit stream and region of interest coding. The bit stream organization increases the options for imagery systems to efficiently parse and decode JPEG2000 images based on the platform targeted by the decoder.

The disadvantage of JPEG2000 is a computational complexity increase of 30 times to encode an image and 10 times to decode an image when compared to the original JPEG standard [5]. The computational difference between the original JPEG standard and JPEG2000 is further magnified by the continuous increase in pixel densities of modern focal plane arrays (FPAs), which only further amplifies the problem. The complexity increase, combined with the parallel nature of the JPEG2000 algorithm, supports the use of application specific integrated circuit (ASIC) or field programmable gate array (FPGA) implementations.

Many designs have been proposed to implement the JPEG2000 decoder using hardware description language (HDL) implementations to be used in FPGAs or in developing ASICs [6–10, 11]. In [7], a column and sample skipping technique is used to speed up decoding while decreasing the quality of the decoded image. In [6] and [11], Handel-C is used to speed hardware development time with the trade-off of a less efficient implementation. While [6] implements the whole decoder in Handel-C, [11] only implements the arithmetic decoder in Handel-C. In [8], a hardware decoder for digital cinema is developed requiring that the images be previously encoded using parallel mode. [10] designs a very large scale integration (VLSI) implementation of the JPEG2000 arithmetic decoder. The design from [9] reduces the latency of the decoder to require one clock cycle to decode a bit by decreasing the clock speed and increasing the amount of logic required.

The JPEG2000 decoder algorithm is profiled in [2, 4], with both concluding that the entropy decoding operation uses the largest percentage of the processing time and the most memory. Thus the entropy decoder is the best candidate for hardware acceleration.

This paper describes a new JPEG2000 binary arithmetic decoder design in the Very High Speed Integrated Circuit Hardware Description Language (VHDL). The results of the new design are compared to various FPGA implementations. It is shown that this new design improves the

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