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High-throughput CAVLC architecture for real-time H.264 coding using reconfigurable devices

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Abstract One of the encoding methods offered by H.264 AVC is context-based adaptive variable length coding (CAVLC). This paper presents a high-throughput hardware implementation of the CAVLC encoder. A dual-coefficient scanning phase is investigated and modified to improve the speed of the encoding phase. This improved scanning solution determines all the required data for the encoding phase to be completed in a minimized and constant number of clock cycles. In addition, an algorithmic approach for encoding levels is exploited to reduce hardware resource requirements. The modified scanning phase approach offers significant throughput capabilities for CAVLC: at 200 MHz, the architecture is capable of encoding 1,080 p video files at 95 fps.

Keywords Context-based adaptive variable length coding (CAVLC) · H.264/AVC · Field Programmable Gate Array (FPGA) · Real-time processing · Entropy encoding

1 Introduction

Variable length code (VLC) plays an important role in the H.264 video compression standard [13]. Many of the codewords used by H.264 are stored in look-up tables (LUTS). Choice of a codeword is based on the frequency of occurrence of the symbol it represents. In H.264, several characteristics and properties of a frame are tracked in order to minimize the length of future codewords. Essentially, each symbol uses multiple VLC tables that are adapted to the symbol's context to create a codeword. This is officially known as context-based adaptive variable length coding, or CAVLC.

The CAVLC encoder is often seen as a bottleneck in the H.264 encoding engine. The encoder requires knowledge of previously encoded data to operate, which limits the number of instances of the CAVLC encoder to one per slice (a fixed portion of a coded video frame). With this limitation, encoding high-definition video (720 and 1,080 p) in real-time requires a high-performance design that is difficult to implement in software. Many engineers have turned to HDL solutions to meet the high-throughput requirements of high-definition encoding [1, 2, 4, 5–11, 14]. These designs vary from small, mobile applications [9] to high-powered, memory-expensive solutions [10].

In this paper, a high-performance implementation of CAVLC is investigated and realized. The design is based on previous architectures, but implements a modified scanning phase that allows for an improved encoding phase. This design is capable of encoding a 16×16 macroblock (MB) in a maximum of 258 clock cycles. At 200 MHz, the proposed implementation can encode one 1,080 p frame in at least 0.0105 s, or a minimum of 95 frames per second. This CAVLC design is intended for use by high-throughput H.264 architectures with wide-area surveillance applications, in which the primary requirement is high frame rate. Its memory requirements are that of most high-throughput architectures, as a result of the arithmetic table elimination techniques use. The proposed architecture also displays relatively low power requirements, consistent with FPGA design.

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