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# Comparative Studies of the Growth and Characterization of Germanium Epitaxial Film on Silicon (001) with 0° and 6° Offcut

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The quality of germanium (Ge) epitaxial films grown directly on silicon (Si) (001) with 0° and 6° offcut orientation using a reduced-pressure chemical vapor deposition system is studied and compared. Ge film grown on Si (001) with 6° offcut presents ~65% higher threading dislocation density and higher root-mean-square (RMS) surface roughness (1.92 nm versus 0.98 nm) than Ge film grown on Si (001) with 0° offcut. Plan-view transmission electron microscopy also reveals that threading dislocations are more severe (in terms of contrast and density) for the 6° offcut. In addition, both high-resolution x-ray diffraction and Raman spectroscopy analyses show that the Ge epilayer on 6° offcut wafer presents higher tensile strain. The poorer quality of the Ge film on Si (001) with 6° offcut is a result of an imbalance in Burgers vectors that favors dislocation nucleation over annihilation.

**Key words:** Germanium, offcut, heteroepitaxy, reduced-pressure chemical vapor deposition

## INTRODUCTION

For the past few decades, rigorous scaling methods have been driving silicon (Si) complementary metal–oxide–semiconductor (CMOS) technology to maintain device performance, decrease power consumption, and reduce cost per transistor.[1,2] As the device size approaches the scaling limit, a paradigm shift has occurred in the industry from dimensional scaling alone to materials innovation. One such example is the compound III–V materials, which have unique properties for future high-speed and low-power computation applications.[3–9] Most of the III–V materials show 20× to 70× higher electron mobility and ~20× higher conductivity compared with Si. In addition, the feasibility of bandgap engineering in III–V materials enables fabrication of devices suitable for communications and optoelectronics applications. However, III–V materials are not able to replace Si completely because the substrates are expensive and smaller in size due to brittleness (wafer diameters are typically less than 200 mm). Therefore, III–V materials have to be integrated onto a Si substrate in order to be compatible with mainstream CMOS manufacturing. To realize III–V materials integration on low-cost, mechanically stronger Si substrates, a number of research groups have investigated III–V growth on Si for optoelectronic and microelectronic applications.[10,11]

The main challenges of producing high-quality III–V materials on Si are: (i) the large lattice mismatch between the two materials [in the case of gallium arsenide (GaAs), the mismatch is 4.1%], and (ii) the formation of antiphase domains (APDs) due to the polar compound semiconductor growth on

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